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JC803 U.S. PTO 08/11/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	06192.0148.NPUS00
First Named Inventor or Application Identifier	PARK
Title	Thin Film Transistor Array Substrate For A Liquid Crystal Display Having Repair Lines
Express Mail Label No.	

JC784 U.S. PTO 09/636466 08/11/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] *Fee Transmittal Form (Form PTO-1082) *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 14] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [*Total Sheets* 4]
4. Oath or Declaration [*Total Pages*]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Two) *(should be specifically itemized)*
14. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [X] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

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17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: /
Prior Application Information: Examiner: Group/Art Unit:

18. CORRESPONDENCE ADDRESS

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August 11, 2000

Box New Applications
Assistant Commissioner for Patents
Washington, DC 20231

Re: New Utility Non-Provisional U.S. Patent Application
Application No. **TO BE ACCORDED** Filed **HEREWITH**
Title: **THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY HAVING REPAIR LINES**
Inventor: **Woon-Yong PARK**
Our Ref: 06192.0148.NPUS00

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. U.S. Utility Patent Application entitled:
THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY HAVING REPAIR LINES

and naming as inventor: **Woon-Yong PARK**

the application consisting of:
a. A specification containing:
(i) **10** pages of description prior to the claims;
(ii) **3** pages of claims (**10** claims);
(iii) a **one** (1) page abstract;
b. **4** sheets of drawings: (**Figures 1, 2, 3 and 4**);

2. Form PTO-SB/05;

3. Form PTO 1082;

4. Certified copy of Korean Patent Application No. 99-33092 claiming priority to August 12, 1999; and

5. Two (2) return postcards

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without filing fee.

Respectfully submitted,

Michael J. Bell
Registration No. 39,604

Enclosures

FORM PTO-1082

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Attorney Docket No. **06192.0148.NPUS00**

ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor: **Woon-Yong PARK**

For: **THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY HAVING REPAIR LINES**

Enclosed are:

☑ 4 sheets of drawings

☑ A certified copy of a Korean Patent Application No. 99-33092.

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
FOR	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$ 345.00	OR		$ 690.00
TOTAL CLAIMS	10-20 =	*	x 9 =		OR	x 18 =	
INDEP. CLAIMS	1-3 =	*	x 39 =		OR	x 78 =	
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+ 130 =		OR	+ 260 =	
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Date 8/11/00

Michael J. Bell
Registration No. 39,604

THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY HAVING REPAIR LINES

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a thin film transistor (TFT) array substrate for a liquid crystal display and, more particularly, to a TFT array substrate having with repair lines.

(b) Description of the Related Art

Generally, liquid crystal displays are structured with a color filter substrate with a common electrode and color filters, a TFT array substrate with TFTs and pixel electrodes, and a liquid crystal sandwiched between the substrates. In operation, different voltages are applied to the common electrode and the pixel electrodes to form electric fields, and under the application of the electric fields, the molecular orientation of the liquid crystal changes. This controls light transmission and displays pictorial images on the screen.

The TFTs are connected to the pixel electrodes individually in order to switch the voltage applied to each pixel electrode.

Gate lines for transmitting scanning signals to the TFTs, and data lines for transmitting pictorial image signals to the TFTs are formed at the TFT array substrate. Such gate and data lines are easy to break or to be disconnected during the device fabricating process. In order to repair such a breakage or

disconnection, repair lines are usually provided at the TFT array substrate.

Conventionally, one or two repair lines are formed at the target data lines or gate lines such that they cross both end portions of the data or gate lines. The repair lines are interconnected via lines formed at tape carrier packages (TCPs) and at a printed circuit board (PCB).

In the TFT array substrate with such repair lines, when lines (for example, data lines) are broken, a laser is irradiated to the crossed portion between the broken line and the repair line and both sides of the broken line are short-circuited by way of the repair line. In this way, pictorial image signals can be transmitted to the disconnected side of the data line via the repair line.

However, when one or two repair lines cross all of the gate lines or data lines, four broken lines may be repaired at most.

In order to repair more broken lines, it has been suggested that the lines connected to one driving integrated circuit (IC) be packaged into one block, and that a separate repair line be formed for each block.

However, such a technique involves several shortcomings.

First, in the usual TCPs, it is difficult to form as many pads as the number of repair lines. Furthermore, as the number of pads increases, the length of the TCPs for the gate driving IC should increase to be connected to the underlying repair lines. Consequently, TCPs having a special structure would be required, resulting in increased production cost. In addition, either as many interconnection lines for the repair lines should be formed at the PCB as the number of driving ICs, or twice as many. Therefore, the volume of the PCB would be increased, resulting in a larger device size.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a TFT array substrate for a liquid crystal display that can be fabricated in a cost-effective manner.

It is another object of the present invention to provide a TFT array substrate for a liquid crystal display of a minimum device size.

These and other objects may be achieved by a TFT array substrate for a liquid crystal display including an insulating substrate with a display area and a peripheral area surrounding the display area. The peripheral area has an upper region above the display area and a lower region below the display area. Signal lines are formed on the substrate such that the signal lines are bundled into a plurality of blocks, and each block has a predetermined number of the signal lines. A plurality of first upper repair lines are formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines, and a plurality of second upper repair lines are formed at the upper peripheral region of the substrate, crossing all of the signal lines. A plurality of first lower repair lines are formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines, and these first lower repair lines cross the signal lines crossed by the first upper repair lines. A plurality of second lower repair lines is formed at the lower peripheral region of the substrate, crossing all of the signal lines. A plurality of upper connection members crosses the first upper repair lines and the second upper repair lines, and a plurality of lower connection members cross the first lower repair lines and the second lower repair lines.

The first upper repair lines and the first lower repair lines may be

interconnected via first dummy pads of TCPs and first interconnection lines of a PCB, and second dummy pads of the TCPs and second interconnection lines of the PCB may be further provided to interconnect the first upper and lower repair lines.

A plurality of third upper repair lines may be formed at the upper peripheral region of the substrate while crossing the upper connection members and all of the signal lines, and a plurality of third lower repair lines may be formed at the lower peripheral region of the substrate while crossing the lower connection members and all of the signal lines.

Each block of the signal lines may include the signal lines connected to one of the ICs, and the first upper and lower repair lines may cross two blocks of the signal lines. The signal lines may be data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a circuit diagram of a TFT array substrate for a liquid crystal display according to a first preferred embodiment of the present invention;

Fig. 2 illustrates the method of repairing broken lines at the TFT array substrate shown in Fig. 1;

Fig. 3 is a circuit diagram of a TFT array substrate for a liquid crystal

display according to a second preferred embodiment of the present invention; and

Fig. 4 illustrates the method of repairing broken lines at the TFT array substrate shown in Fig. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a circuit diagram of a TFT array substrate for a liquid crystal display according to a first preferred embodiment of the present invention.

As shown in Fig. 1, a plurality of data lines 12 is formed on an insulating substrate 10 in the vertical direction. A plurality of gate lines (not shown) is formed on the substrate 10 in the horizontal direction. The data lines 12 cross the gate lines to thereby form a display area 11 where pictorial images are displayed. The substrate 10 has a peripheral area externally surrounding the display area 11. The peripheral area may be roughly divided into left, right, upper and lower regions with respect to the display area 11.

Driving ICs 20 and 30 are provided at the upper and left peripheral regions of the substrate 10 such that they are connected to the data lines 12 and the gate lines, respectively. The driving ICs 20 and 30 are mounted on the substrate 10 via TCPs, and dummy pins 21, 22, 31 and 32 are formed at the sides of the driving ICs 20 and 30.

Three kinds of repair lines are formed at the upper and lower peripheral regions of the substrate 10 such that they cross the data lines 12 while being

insulated therefrom.

A set of three first repair lines 41 and another set of three first repair lines 42 are formed at the upper and lower peripheral regions respectively. The first repair lines 41 and 42 cross only the data lines 12 connected to two of the data driving ICs 20. The upper and lower repair lines 41 and 42 cross the same data line 12 as a pair. Of course, the number of the first repair lines 41 and 42 may be increased or decreased depending upon the number of the driving ICs. Furthermore, the first repair lines 41 and 42 may cross other than the data lines 12 connected to the two data driving ICs 20, if necessary.

The second repair line 43 and the third repair line 44 are formed at the upper peripheral region of the substrate 10, and the second repair line 45 and the third repair line 46 are formed at the lower peripheral region of the substrate 10, and they cross all of the data lines 12.

Furthermore, connection members 47 are formed at the substrate 10, crossing the first to third upper repair lines 41, 43 and 44 at the upper peripheral region, and at the first to third lower repair lines 42, 45 and 46 at the lower peripheral region. The number of the connection members 47 is as many as the number of the first repair lines 41 and 42, but may be increased as needed. For example, there may be as many connection members 47 as there are driving ICs 20.

Each pair of first upper and lower repair lines 41 and 42 formed at the upper and lower peripheral regions of the substrate 10 is interconnected via interconnection lines 50 formed at the PCB. The first repair lines 41 and 42 are linked to the interconnection lines 50 formed at the PCB via the dummy pins 21,

22 and 32 of the driving ICs, and dummy pads formed at the TCPs.

The first upper repair lines 41 are connected to all of the dummy pins 21 and 22 of the driving ICs 20 connected to the data lines 12 that they cross. The dummy pins 21 and 22 are bundled, and linked to the interconnection lines 50.

In the above structure, the number of interconnection lines 50 for interconnecting the upper and lower repair lines is significantly reduced so that the volume of the PCB can be minimized while decreasing the number of dummy pads for drawing the repair lines. This makes it possible to use common TCPs.

A signal amplifying circuit (not shown) may be added in the interconnection line 50 to compensate for signal retardation through amplifying the pictorial signals transmitted along the interconnection line 50.

Fig. 2 illustrates the method of repairing broken data lines at the TFT array substrate where two of the data lines 12 connected to one driving IC 20 are broken (at the A and a portions).

First, a laser beam is irradiated to the crossing points B and C between the first upper and lower repair lines 41 and 42 and the data line 12 broken at the A portion, and short-circuits them. As a result, the pictorial image signal started from the driving IC 20 is transmitted to the first upper repair line 41 at the short circuited portion B, and transmitted to the first lower repair line 42 via the dummy pad and dummy pin 21 of the TCP, and the interconnection line 50 of the PCB. The pictorial image signal is then transmitted to the side of the data line 12 below the broken portion A thereof via the short-circuited portion C.

In the meantime, the crossed portions b and e between the third upper and lower repair lines 44 and 46 and the data line 12 broken at the a portion, the crossing points d and g between the first repair lines 41 and 42 not crossing the data line 12 broken at the a portion and the connection members 47, and the crossed portions c and f between the connection members 47 and the third repair lines 44 and 46 are irradiated by a laser beam, and short-circuited. In this case, the pictorial image signal started from the data driving IC 20 is first transmitted to the neighboring first upper repair line 41 via the short-circuited portions b, c and d. Then, the pictorial image signal is transmitted to the neighboring first lower repair line 42 via the interconnection line 50 of the PCB. Consequently, the pictorial image signal is transmitted to the side of the data line 12 below the broken portion a via the short-circuited portions g, f and e. At this time, the first repair lines 41 and 42 to be connected to the third repair lines 44 and 46 via the connection members 47 are selected from those that do not cross the broken data lines 12.

In the above structure, even though the breakage of the data lines 12 are concentrated at a particular area, the broken lines can all be repaired using the neighboring spare repair lines and the appropriate interconnection line efficiently.

Fig. 3 is a circuit diagram of a TFT array substrate according to a second preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the TFT array substrate are similar to those related to the first preferred embodiment except that two interconnection lines 51 and 52 are used to interconnect the first upper and

lower repair lines 41 and 42. The two interconnection lines 51 and 52 are linked to the left and right end portions of the first repair lines 41 and 42, respectively.

Fig. 4 illustrates the method of repairing breakage of the data lines 12 at the TFT array substrate shown in Fig. 3 where three broken portions A, a and α are exemplified. The method of repairing the broken portions A and a is similar to the first preferred embodiment. In order to repair the broken portion α, the crossed portions between the data line 12 broken at the α portion and the upper and lower first repair lines 41 and 42 are short-circuited. Thereafter, the X portions between the short-circuited portions β and B, and γ and C of the first repair lines 41 and 42 are cut using a laser. In this case, the disconnected upper and lower portions of the three broken data lines 12 are interconnected via the route indicated by the dotted line in the drawing.

In the case of broken gate lines, the same technique can be employed for repairing them.

As described above, even though line breakage is concentrated at a particular area, such line breakages can all be repaired using the spare neighboring repair lines and the interconnection lines efficiently. Therefore, the number of interconnection lines can be significantly reduced while minimizing the volume of the PCB. Furthermore, the number of dummy pads for drawing the repair lines can also be reduced while making it possible to use common TCPs.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that

various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate with a display area and a peripheral area surrounding the display area, the peripheral area having an upper region above the display area and a lower region below the display area;

signal lines formed on the substrate such that the signal lines are bundled into a plurality of blocks, each block having a predetermined number of signal lines;

a plurality of first upper repair lines formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines;

a plurality of second upper repair lines formed at the upper peripheral region of the substrate, crossing all of the signal lines;

a plurality of first lower repair lines formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines, the first lower repair lines crossing the signal lines crossed by the first upper repair lines;

a plurality of second lower repair lines formed at the lower peripheral region of the substrate, crossing all of the signal lines;

a plurality of upper connection members crossing the first upper repair lines and the second upper repair lines; and

a plurality of lower connection members crossing the first lower repair lines and the second lower repair lines.

2. The thin film transistor array substrate of claim 1, further

comprising:

a plurality of first interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

3. The thin film transistor array substrate of claim 2, wherein the first upper repair lines are drawn from two or more dummy pins of integrated circuits for driving the signal lines, and are linked to the first interconnection lines.

4. The thin film transistor array substrate of claim 2, further comprising:

a plurality of second interconnection lines interconnecting the first upper repair lines and the first lower repair lines.

5. The thin film transistor array substrate of claim 1, further comprising:

a plurality of third upper repair lines formed at the upper peripheral region of the substrate while crossing the upper connection members and all of the signal lines; and

a plurality of third lower repair lines formed at the lower peripheral region of the substrate while crossing the lower connection members and all of the signal lines.

6. The thin film transistor array substrate of claim 1, wherein each block of the signal lines comprises the signal lines connected to one of the integrated circuits.

7. The thin film transistor array substrate of claim 6, wherein the first upper and lower repair lines cross two blocks of the signal lines.

8. The thin film transistor array substrate of claim 7, wherein one or more of the upper and lower connection members are formed at each block of the signal lines.

9. The thin film transistor array substrate of claim 4, wherein the first and second interconnection lines are formed on a printed circuit board.

10. The thin film transistor array substrate of claim 4, further comprising:

a signal amplifying circuit in the first and second interconnection lines.

ABSTRACT OF THE DISCLOSURE

A thin film transistor array substrate for a liquid crystal display includes an insulating substrate with a display area and a peripheral area surrounding the display area. The peripheral area has an upper region above the display area and a lower region below the display area. Signal lines are formed on the substrate such that the signal lines are bundled into a plurality of blocks. Each block has a predetermined number of signal lines. A plurality of first upper repair lines is formed at the upper peripheral region of the substrate, crossing one or more blocks of the signal lines. A plurality of second upper repair lines is formed at the upper peripheral region of the substrate, crossing all of the signal lines. A plurality of first lower repair lines are formed at the lower peripheral region of the substrate, connected to the corresponding first upper repair lines. The first lower repair lines cross the signal lines crossed by the first upper repair lines. A plurality of second lower repair lines is formed at the lower peripheral region of the substrate, crossing all of the signal lines. A plurality of upper connection members crosses the first upper repair lines and the second upper repair lines. A plurality of lower connection members crosses the first lower repair lines and the second lower repair lines. In this structure, even though line breakage is concentrated at a particular area, such line breakage can be collectively repaired using the spare neighboring repair lines and interconnection lines interconnecting the repair lines efficiently.

FIG. 1

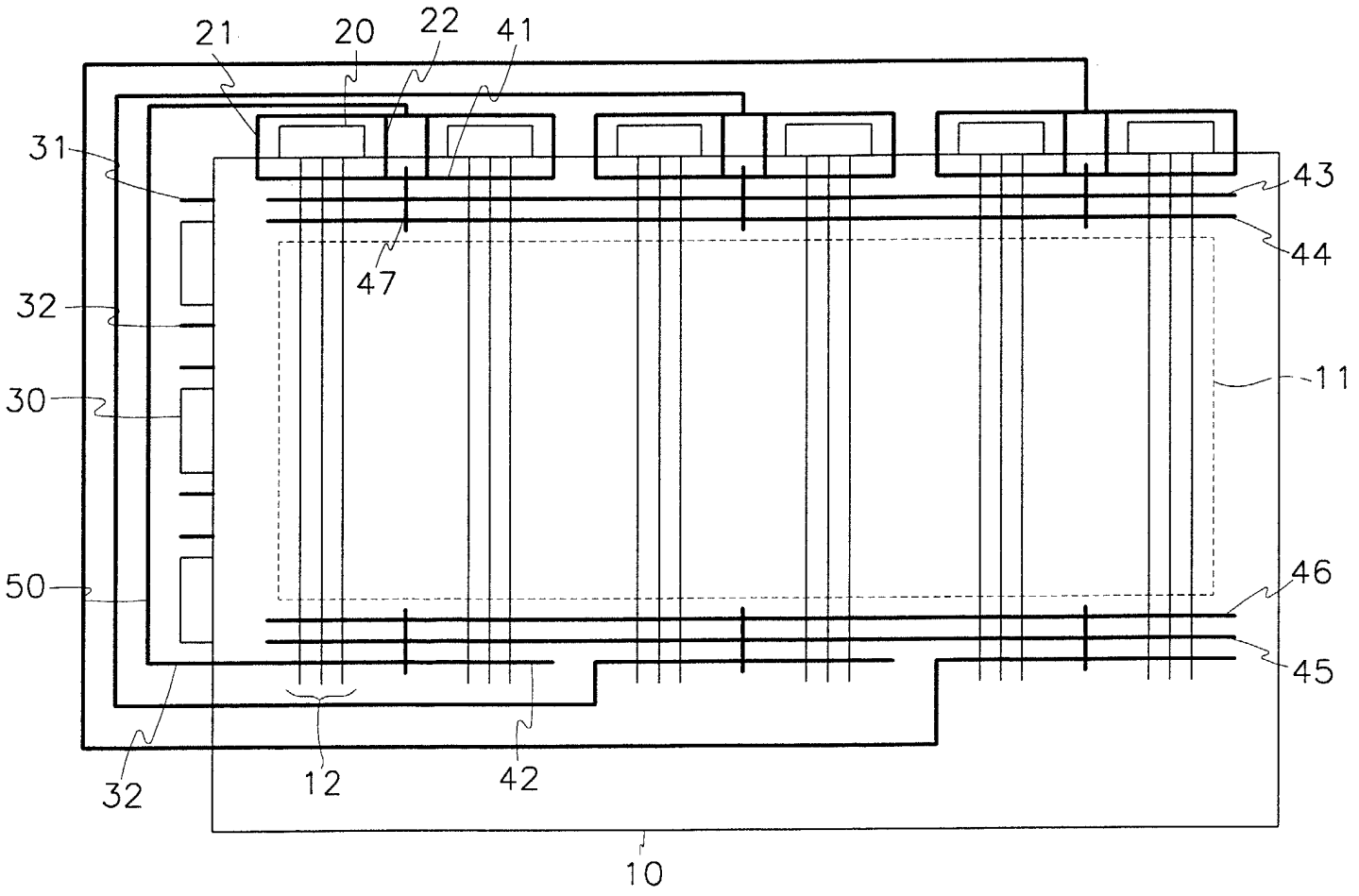

FIG.2

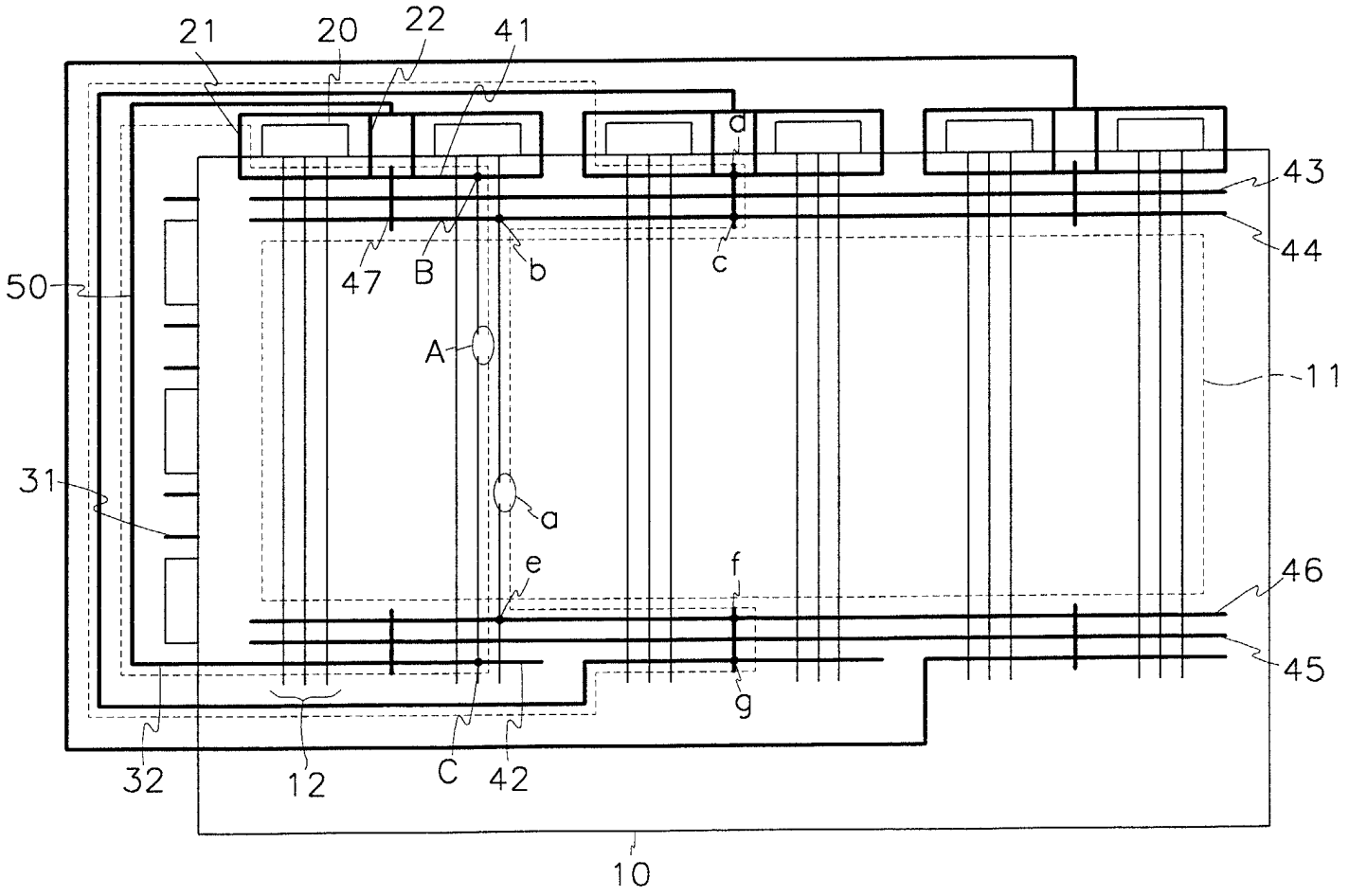

FIG.3

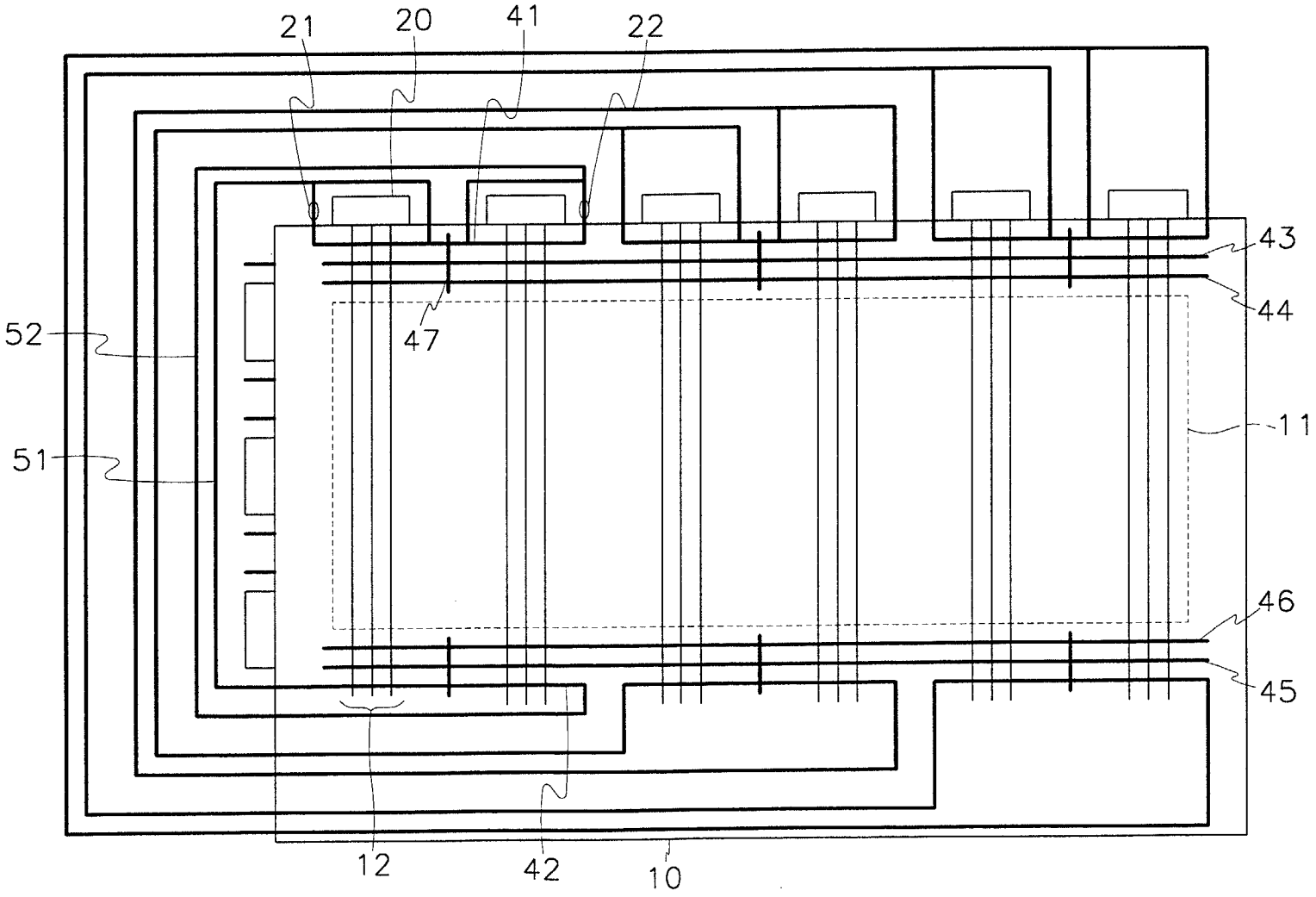

FIG.4